AND8341/D

ADC Offset Calibration of the BelaSigna® 300 Series

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APPLICATION NOTE

Introduction

This application note explains the way the Analog−to−Digital Converters (ADCs) on BelaSigna 300 are calibrated, and why this calibration is recommended. The intended audience is customers building applications using the BelaSigna 300 WLCSP chip who need to calibrate BelaSigna 300 at the production line. In this case, the SPI EEPROM attached to BelaSigna 300 will be loaded with the ADC calibration values. To accomplish this, a calibration script is provided.

BelaSigna 300 features 4 ADC channels. Each of these channels has 8 possible gain settings, for a total of 32 values for complete calibration. Calibrating each of these settings is done independently of the others. All development boards shipped from ON Semiconductor come with all 32 values pre−calibrated, however, when producing an assembly featuring BelaSigna 300, it will be more efficient to only calibrate the settings that are used in a given design.

The main goal of this application note is to describe how the calibration should be performed, and what should be taken into account to ensure proper calibration. It is not intended to provide deep technical explanations on the DC offset effects. However, more details on how the DC offset impacts the audio quality can be found in Appendix A of this application note.

TYPES OF CALIBRATION SCRIPTS

Default Calibration Script

This type of calibration will calibrate all possible preamp settings for the 4 channels. This will be done on EDK hardware shipped out of ON Semiconductor. The default calibration script is available on the extranet. Please visit https://extranet.my.amis.com/ to access the script. Note that this script requires/ assumes a 38.4 MHz clock.

Custom Calibration Script

This type of calibration will involve calibrating only the channels and preamp which will be used in the application. This type of calibration script is generated upon request from the customer to minimize the time which will take to calibrate BelaSigna 300. If you require a custom calibration script, please contact ON Semiconductor with information about your settings for more information. See the end of this application note for contact details.

CONCEPT AND PROCEDURE

Relationship between the DC Offset and the Noise Hump

BelaSigna 300 is realized in 130 nm technology, and the operational amplifiers (op−amps) designed in this technology produce DC offset values that can produce audible baseband artifacts when accumulated in the closed loop of an ADC converter. This may result in some bumps or spikes in the noise floor that are audible. These artifacts may make the noise floor sound like a waterfall or another undesirable sound rather than like pleasant white noise.

The Sigma Delta structure of the ADCs of BelaSigna 300 includes feedback loops. In 130 nm technology, the operational amplifiers will produce a certain offset, and the action of these feedback loops will produce an oscillation on the ADC output. In order to handle this effect, the amount of DC offset must be modified such that this oscillation does not create any artifacts in the audio bands. The value of this DC offset is configurable using a dedicated register, which is comprised of one setting for each of the eight preamp settings in each of the four channels.

DC Offset Registers and Calibration

Each channel of the input stage has its own DC offset register. The value for the DC offset will depend on the analog gain that is applied by each channel's preamplifier. The possible gains applied are 0, 12, 15, 18, 21, 24, 27 and 30 dB, which makes a total of 8 possible gain settings per channel. Since we have 4 channels, a total of 32 DC offset values should be measured.

Each DC offset value is coded in an 8−bit field that corresponds to 255 different DC offset levels (both positive and negative). The 8−bit value is formatted as sign−magnitude, where a larger positive value will produce a higher positive DC offset (and a larger negative number will produce a more negative DC offset). One single 32−bit register is made up of the four calibration values, and is located in P−Memory at address 0xE14F. The calibration

values for the DC offset should be stored in the manufacturing area of the EEPROM that is attached to BelaSigna 300. For more details on the EEPROM file system of BelaSigna 300, please refer to Chapter 7 of the Firmware Reference Manual.

In order to calibrate the DC offset for BelaSigna 300, a certain calibration procedure should be run on each piece. Your ON Semiconductor Field Application Engineer will provide you with the calibration scripts, programs and guidelines needed to properly configure BelaSigna 300. Note that the DC offset calibration values are not the only values that needs to be calibrated on each individual piece: indeed, the internal oscillator as well as the VDDC supply should be calibrated too, and the calibration results should be stored in the EEPROM in locations according to the file system. Putting the necessary calibration values in the proper locations in EEPROM allows the firmware macros to access and load the calibration values, resulting in optimal system behavior.

A calibration script for DC offset provides an automated mechanism to determine the DC offset value for each ADC and each preamplifier gain that will result in a clean, flat noise floor. This procedure consists of two parts: firstly measuring the amount of DC accumulated in the input stage (which is fabrication process dependant), and then secondly finding the correct calibration register value such that the DC offset will be in a desired range of acceptable values.

At boot, using the standard sk3 bootloader, the 33 bytes are copied from the Manufacturing Area of the EEPROM to low Y−memory. These 33 bytes represent the 32 DC offset values ((8 preamplifiers x 4 ADCs) plus a status byte). The calibration values are packed into 11x 24−bit (3 byte) words. Then, in the final application, when the preamplifier settings are changed, the Sys_Set_IN_GAIN_CTRL macro will change the preamplifier gain and will also copy the corresponding DC offset value from its location in the Y memory to the DC offset calibration register (PMEM: 0xE14F),

The calibration scripts use a library called sk3_dcOffsetCal was created and it encapsulates all the necessary functions to calibrate and save the values in the EEPROM file system. More details on the library can be found in Appendix B of this application note. This library can be incorporated with the production test to ensure a clean noise floor.

APPENDIX A

Relationship Between Audio Quality and DC Offset

This appendix is provided for those who wish to understand the background behind the ADC calibration procedure but it is not critical for performing the calibration to read this section. There is a relationship between the DC offset magnitude, and the ADC output oscillation. BelaSigna 300 uses a sigma delta conversion technique that includes feedback loops. Through this structure, a small amount of generated DC offset corresponds to a slow ADC output oscillation (large period between 2's complement wrap around), and a large amount of DC offset corresponds to a fast ADC output oscillation (small period between 2's complement wrap around). Figure 1 shows the correlation between the DC offset and the speed of oscillation.

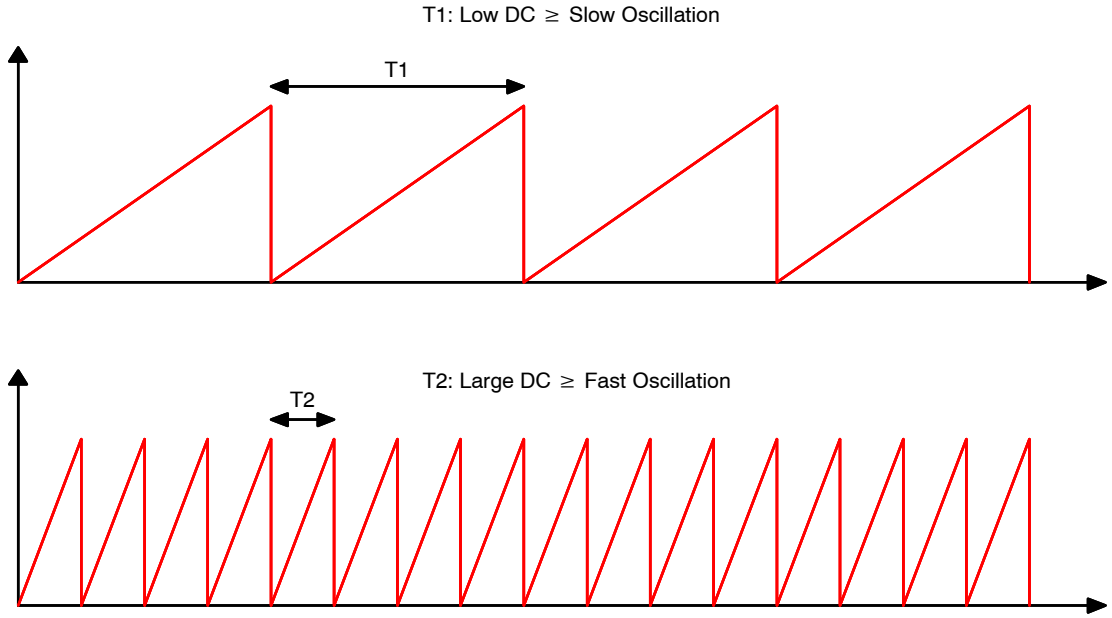

Figure 1. Correlation between DC Offset and Oscillation Frequency

The noise hump is directly related to the ADC output oscillation. In fact, the observed noise hump will have a center frequency equal to the frequency of the ADC output oscillation, or 1/T (where T is the period of time required for the 2's complement to wrap around). As a result, a small DC offset corresponds to a slow output oscillation (large period), which in turn corresponds to a frequency, which may be under 8 kHz, and hence will become present in baseband as a hump (such as T1 in the figure below).

The goal of the calibration is to prevent the hump from appearing in the baseband. To do this, the offset should be tuned so that the ADC output frequency will be somewhere between the 8 kHz band and any alias band. This is illustrated in the Figure 2 below.

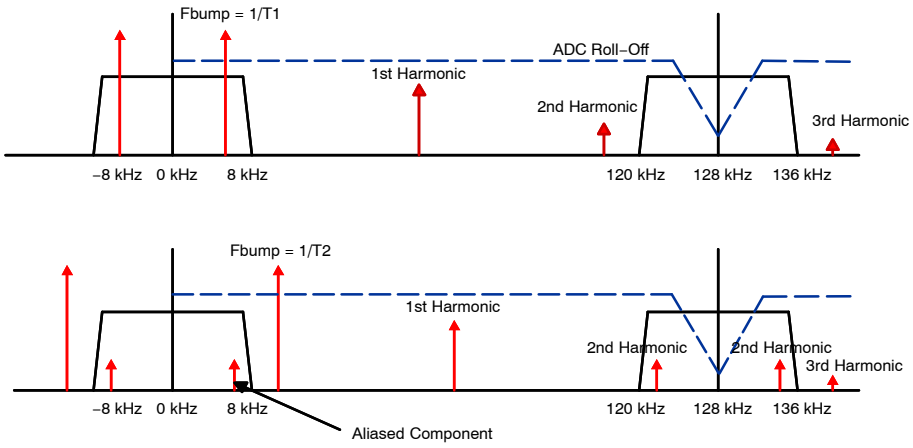

Figure 2. ADC Output Oscillation Frequency Placement

Since the actual sample rate is 8x the base sample rate, there will be an alias band centered at the frequency 8 * 16 kHz = 128 kHz, with bands of ±8 kHz around this center frequency. All humps that land within an alias band can potentially lead to a hump in the base band. Figure 3 shows the ADC offset region that will lead to a hump in the audio band.

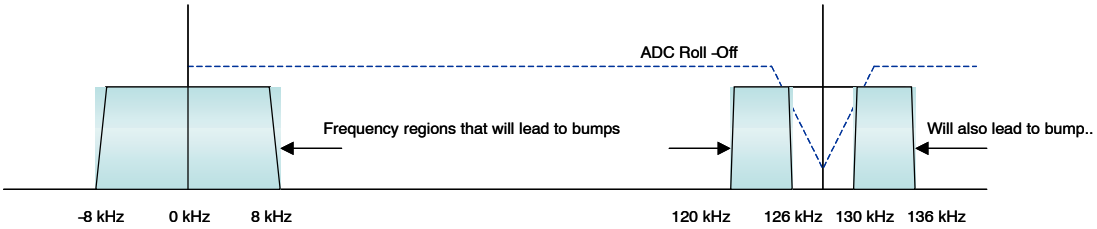

Figure 3. Frequency Regions that Will Lead to Humps

The relationship between the ADC output frequency and DC offset is known. The purpose of the DC offset calibration is to ensure that the DC offset corresponds to an ADC output frequency that is out of the above mentioned band, and this is what is done during the calibration process. The known good regions are shown in Figure 4 below. From the data, the lowest amount of DC that will produce an ideal noise floor is 14.65 mV, with a maximum tolerance of ±8.75 mV.

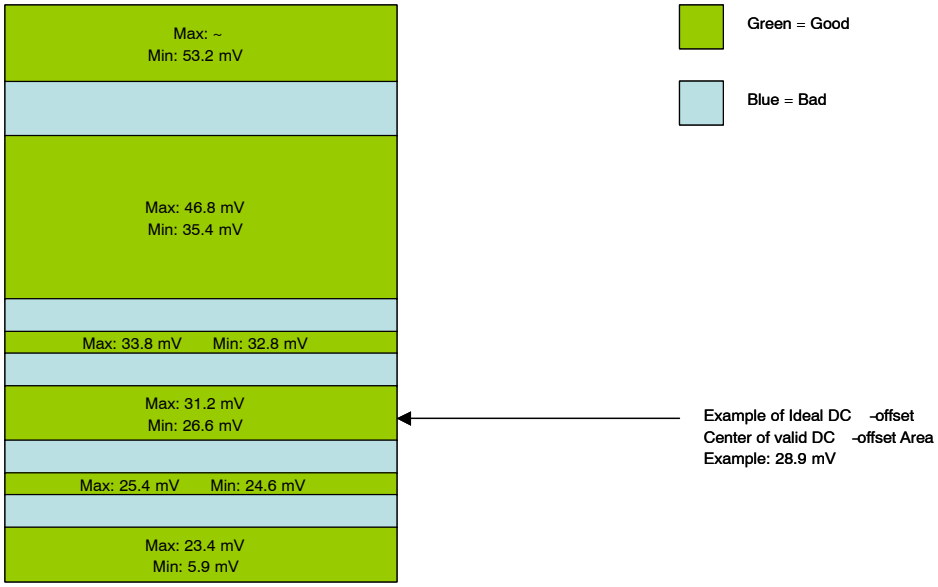

Figure 4. DC Offset Value Mapping to Frequency Good/Bad Frequency Ranges

APPENDIX B

Sk3_dcOffsetCal Library

To make use of this library, all that is required is to include the header file (dcOffsetCal.cfi) in your project, and instruct the linker to link with the .lib file.

The library consists of five user definable variables, and ten functions (including an ISR).

User Defined Variables

TARGET_DC_OFFSET

This variable instructs the algorithm, which target DC offset is expected to be obtained. To convert voltage to the required quantity, simply multiply the desired DC offset (in volts) by 2^17 (131,071)

TARGET_ACCURACY

This variable is used to determine how close the calibrated DC offset should be to the TARGET_DC_OFFSET (essentially error magnitude). To convert voltage to the required quantity, simply multiply the desired tolerance (in volts) by 2^17 (131,071).

MAX_ITERATIONS

This variable is used to instruct the algorithm the number of iterations to go through before giving up. The algorithm will stop once a solution within the target accuracy is found, or this number of iterations has been tried).

DID_NOT_CONVERGE_BIT

To provide a means to indicate that this value did not converge within the desired accuracy after the maximum number of iterations, a flag bit will be set in the calibration value at this location to indicate such.

Functions

dcOffsetCal_Init

The function dcOffsetCal_Init configures the system so the remaining DC offset functions will work. This function expects the user to only have configured the sampling frequency before calling. The following actions are done by this function:

- Disable the DC Remove filters in the decimation stage
- Configure FIFO A0 (which will be used by the other functions)
- Configure the ISR vector table to run the included ISR on A0 events
- Enable only the A0 interrupt

Throughout the calibration, the IOC will be configured to tie the desired input channel to FIFO A0. This can be done manually, or by *dcOffset_calibrateCompleteSystem()* which will sweep through all possible 32 input channel configurations.

dcOffsetCal_selectADC

This function allows the user to easily select and configure an ADC input channel. The dcOffsetCal_selectADC function will configure the ADC channel, and configure the IOC to pass the data to FIFO A0. An ADC selection value is to be passed into register x0 as input. Valid inputs are *SELECT_ADC[0|1|2|3]*.

dcOffsetCal_selectPreamp

This function allows the user to easily select and configure an Preamp gain setting. The dcOffsetCal_selectPreamp function will configure the Preamplifier to the desired gain. A Preamp Gain selection value is to be passed into register x0 as input. Valid inputs are *SELECT_PREAMP_[0DB|12DB|15DB|18DB|21DB|24DB|27DB|30DB]*

dcOffsetCal_measureDCOffset

The function dcOffsetCal_measureDCOffset takes a reading of the DC offset resulting due to the current configuration. The function requires 96x16 samples to complete, as required for the internal DC and digital filter output to reach steady state. The output is returned in register x0.

dcOffsetCal_calibrateCurrentConfiguration

The function dcOffsetCal_calibrateCurrentConfiguration attempts to find a calibration value for the current configuration using the described algorithm. The calibration value (along with the DID_NOT_CONVERGE_BIT) will be returned in a0.

dcOffsetCal_calibrateCompleteSystem

The function dcOffsetCal_calibrateCompleteSystem sweeps through all 32 possible input channels and preamplifier settings. This function takes an input x−memory location as to where the 32 words should be stored. The parameter is passed to the function through register xp0.

dcOffsetCal_saveToYMem

The function dcOffsetCal_saveToYMem takes a calibration table of 32 words generated by dcOffsetCal_calibrateCompleteSystem, and compresses the calibration values into 10 words saving them to SYSVAR_Y_ADCCAL_START. Once saved to this location, calibration values may be loaded using the SYSLIB_CalibrateADCs function. The 32 word calibration table location is passed to dcOffsetCal_saveToYMem through register xp0.

dcOffsetCal_generatePlotData

The function dcOffsetCal_generatePlotData takes the current input configuration, and sweeps through all 255 possible calibration values, measuring the resulting DC offset produced. This function allows the user to measure the DC offset curve. This function takes an input x−memory location as to where the 255 words should be stored. The parameter is passed to the function through register xp0. The sweep will start from the most negative value, and increment all the way to the most positive value.

dcOffsetCal_ISR

The dcOffsetCal_ISR handles the input data, and implements the digital filter. It is expected to read data from FIFO A0, and run every 16 samples. The ISR is

automatically configured and installed by the dcOffsetCal_Init function.

dcOffsetCal_UpdateMDA

The dcOffsetCal_UpdataMDA replaces the 32 calibration values in the filesystem (and ensures the status byte is set to 0x80) with 32 new calibration values. The input is to be formatted the same way the output of dcOffsetCal_calibrateCompleteSystem is formatted. One calibration value per word, over 32 words is expected. This function reads the entire MDA, updates the calibration values, updates the CRC, and then writes the changes to the filesystem. An input x−memory location as to where the 32 calibration values are stored is to be passed to this function.

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